



## SMTS Logic Design

[Rambus](#) Aix-en-Provence, Provence-Alpes-Côte d'Azur, France



Rambus, a premier chip and silicon IP provider, is seeking to hire a motivated full-time Design engineer to join our IP / PCIe CXL team in Aix-en-Provence, France. Candidates will be joining

some of the brightest inventors and engineers in the world to develop products that make data faster and safer.

As a Design Integrator and tester, the candidate will be reporting to the PCIe IP Design Manager. This full-time position will allow the candidate to develop reference designs to show the potential of the IP, to simulate it and to prototype it on cutting edge FPGAs.

Rambus offers a flexible work environment, embracing a hybrid approach. We encourage employees to spend an average of at least three days per week working onsite, allowing for two days of remote work.

### **Responsibilities**

- Define reference design / example architectures to best demonstrate features of Rambus PCIe / CXL controller IP
- Develop (Verilog) these designs
- Perform simulation with various simulators
- Perform FPGA synthesis implementation flow
- Perform HW Test and debug on cutting edge platforms
- Scripting for continuous integration and automation

### **Qualifications**

Required:

- RTL coding : Verilog / VHDL
- Master's degree or PHD in Electrical Engineering, Computer Engineering or equivalent.
- Good English skills, communication skills, and willingness to work with an international team.

### **Additional Desirable Skills**

- RTL Simulation : Questa / VCS / NCSIM
- FPGA flows : Vivado / Quartus
- CI : Python / Jenkins / GIT

## About Rambus

Rambus is a global company that makes industry-leading memory interface chips and Silicon IP to advance data center connectivity and solve the bottleneck between memory and processing. With over 30 years of semiconductor experience, we are a leading provider of high-performance products and innovations that maximize the bandwidth, capacity and security for AI and other data-intensive workloads. Our world-class team is the foundation of our company, and our innovative spirit drives us to develop the cutting-edge products and technologies essential for tomorrow's systems.

Rambus offers a competitive compensation package, including base salary, bonus, equity and employee benefits.

Rambus is committed to cultivating a culture where we actively seek to understand, respect, and celebrate the complex and rich identities of ourselves and others. Our Diversity, Equity, and Inclusion initiatives are geared towards valuing the differences in backgrounds, experiences, and thoughts at Rambus to help enhance collaboration, teamwork, engagement, and innovation. At Rambus, we believe that we can be our best when every member of our organization feels respected, included, and heard.

Rambus is proud to be an Equal Employment Opportunity and Affirmative Action employer. We do not discriminate based upon race, religion, color, national origin, sex (including pregnancy, childbirth, or related medical conditions), sexual orientation, gender identity, gender expression, age, status as a protected veteran, status as an individual with a disability, genetic information, or other applicable legally protected characteristics.

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## SMTS Validation Engineering

[Rambus](#) Aix-en-Provence, Provence-Alpes-Côte d'Azur, France



Rambus, a premier chip and silicon IP provider, is seeking to hire a motivated full-time Design Integrator and Tester to join our PCIe / CXL Validation team in Aix-en-Provence, France. Candidates will be joining some of the brightest inventors and engineers in the world to develop products that make data faster and safer.

As a Design Integrator and tester, the candidate will be reporting to the Hardware Validation Manager. This full-time position will allow the candidate to develop reference design for Rambus IPs, custom designs for customers' needs and innovative demos for trade shows. The role will involve simulation of the designs, synthesis, timing closure and integration in Hardware using cutting edge FPGA (Agilex-I / Versal Premium) pushed to their limit. This also involves in-system debug on advanced server platforms.

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**Responsibilities:**

- Define reference design / example architectures to best demonstrate features of Rambus PCIe / CXL controller IP
- Develop (Verilog) these designs
- Perform simulation with various simulators
- Perform FPGA synthesis implementation flow
- Perform HW Test and debug on cutting edge platforms
- Preparation for PCIe and CXL compliance Workshops and represent Rambus on those Workshops.
- Development (RTL, Hardware, software, mechanics) of innovative demos and represent Rambus on Tradeshow
- Enhancement of Hardware Validation infrastructure integrating next gen PCIe/CXL systems

**Requirements/Qualifications:**

Required:

- Electrical science, Computer science or equivalent.
- Experience with RTL Design in FPGA and hardware integration
- Good English skills, communication skills, and willingness to work with an international team.

Additional Desirable skills

- Timing closure, debugging : Verilog (Quartus/Vivado)
- RTL Simulation : Questa / VCS / NCSIM
- FPGA flows : Vivado / Quartus
- CI : Python / Jenkins / GIT
- CAD : CADSTAR

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## SMTS Software Development

[Rambus](#) Aix-en-Provence, Provence-Alpes-Côte d'Azur, France



Rambus, a premier chip and silicon IP provider, is seeking to hire a motivated full-time Software engineer to join our Software team in Aix-en-Provence, France. Candidates will be joining some of the brightest inventors and engineers in the world to develop products that make data faster and safer.

As a Software developer, the candidate will be reporting to the Software Lead. This full-time position will allow the candidate to develop software projects around PCIe and CXL ecosystems in collaboration with hardware, verification, and validation engineers. The role will involve software implementation, but also documentation, validation, and internal training.

Rambus offers a flexible work environment, embracing a hybrid approach. We encourage employees to spend an average of at least three days per week working onsite, allowing for two days of remote work.

## **Responsibilities**

- Define and implement new software tools to optimize R&D activities:
- Discuss with the R&D teams to identify areas of improvement.
- Choose the best solutions to match the needs. Explore new frameworks or already top-ranked solutions
- Implement your ideas
- Deploy these new developed tools, teach to the teams how they make the R&D life simpler
- Validate and document your solutions.
- Maintain and improve the software tools already developed by the software team for internal and external users
- Add new features according to the user needs and your new ideas
- Fix the bugs, improve the quality, and tackle the technical debt
- Provide help and support to the users
- Provide a first level of support between the R&D team and the local IT/infrastructure team

## **Qualifications**

Required:

- High skills in C/C++ and Python
- Strong experience in version control systems (Git)
- Strong experience in Continuous Integration (Jenkins).
- Good English skills, communication skills, and willingness to work with an international team.

## **Additional Desirable Skills**



- Good knowledge of Web technologies (Vue.JS, Javascript, HTML/CSS)
- Experience of Django framework
- Good Linux skills (filesystem, network, services)

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